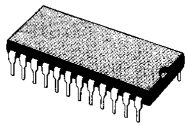
SGS-THOMSON
MICROELECTRONICS

ETL9410/ETL9411
ETL9310/ETL9311

NMOS MICROCONTROLLERS

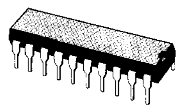
- LOW COST
- POWERFUL INSTRUCTION SET
- 512 x 8 ROM, 32 x 4 RAM
- 19 I/O LINES ETL9410
- TWO-LEVEL SUBROUTINE STACK
- 16μs INSTRUCTION TIME
- SINGLE SUPPLY OPERATION (4.5 - 6.3V)
- LOW CURRENT DRAIN (6mA max.)
- INTERNAL BINARY COUNTER REGISTER WITH MICROWIRE® SERIAL I/O CAPABILITY
- GENERAL PURPOSE AND TRI-STATE® OUTPUTS
- LSTTL/CMOS COMPATIBLE IN AND OUT
- DIRECT DRIVE OF LED DIGIT AND SEGMENT LINES
- SOFTWARE/HARDWARE COMPATIBLE WITH OTHER MEMBERS OF ET9400 FAMILY
- EXTENDED TEMPERATURE RANGE DEVICE ETL9310 ETL9311 (– 40°C to + 85°C)
- WIDER SUPPLY RANGE (4.5 – 9.5V) OPTIONALLY AVAILABLE
- SOIC 20 PACKAGE AVAILABLE

ETL9410/ETL9310



N
(Plastic Package)

ETL9411/ETL9311



N
(Plastic Package)

DESCRIPTION

The ETL9410 and ETL9411 Single-Chip N-Channel Microcontrollers are fully compatible with the COPS® family, fabricated using N-channel, silicon gate MOS technology. The Controller Oriented Processors are complete microcomputers containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The ETL9411 is identical to the ETL9410, but with 16 I/O lines instead of 19. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Controller Oriented Processor at a low end-product cost.

The ETL9310 and ETL9311 are exact functional equivalents but extended temperature versions of ETL9410 and ETL9411 respectively.

PIN CONNECTIONS

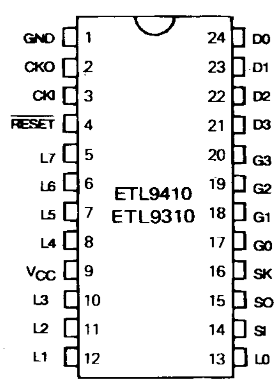
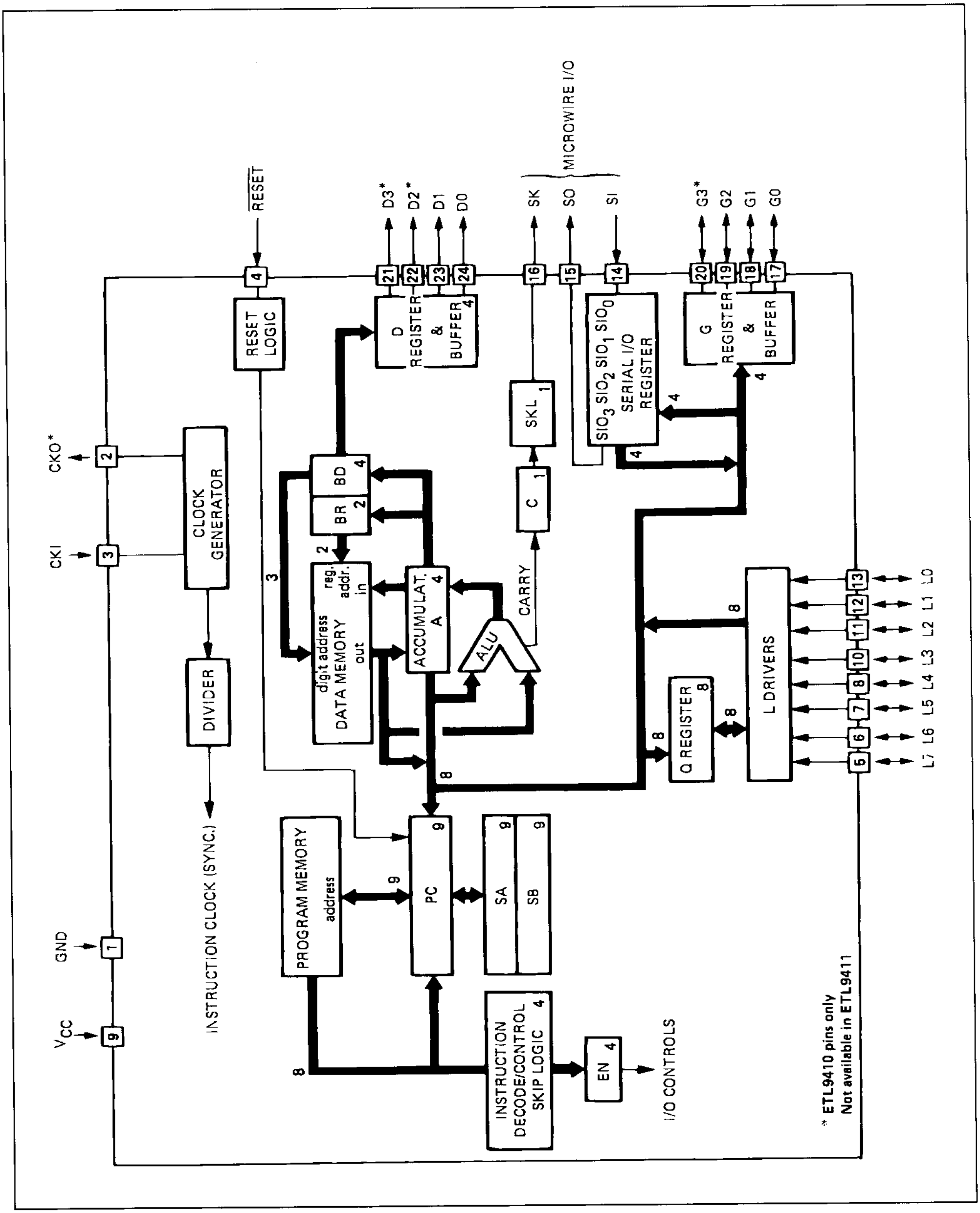


Figure 1 : Block Diagram (24-pin version).



ETL9410/ETL9411

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	Voltage at Any Pin Relative to GND	– 0.5 to + 10	V
	Ambient Operating Temperature	0 to + 70	°C
	Ambient Storage Temperature	– 65 to + 150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C
	Power Dissipation ETL9410 ETL9411	0.75W at 25°C 0.4W at 70°C 0.65W at 25°C 0.3W at 70°C	
	Total Source Current	120	mA
	Total Sink Current	100	mA

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +70°C$, $4.5V \le V_{CC} \le 9.5V$ (unless otherwise specified)

Parameter	Test Conditions	Min.	Max.	Unit
Standard Operating Voltage (V_{CC})	Note 1	4.5	6.3	V
Optional Operating Voltage (V_{CC})		4.5	9.5	V
Power Supply Ripple	Peak to Peak		0.5	V
Operating Supply Current	All Inputs and Outputs Open		6	mA
Input Voltage Levels				
CKI Input Levels				
Ceramic Resonator Input (÷ 8)				
Logic High (V_{IH})		2.0		V
Logic Low (V_{IL})		– 0.3	0.4	V
Schmitt Trigger Input (÷ 4)				
Logic High (V_{IH})		0.7 V_{CC}		V
Logic Low (V_{IL})		– 0.3	0.6	V
$\overline{RESET}$ Input Levels	(schmitt trigger input)			
Logic High		0.7 V_{CC}		V
Logic Low		– 0.3	0.6	V
SO Input Level (test mode)	Note 2	2.0	2.5	V
All Other Inputs				
Logic High	V_{CC} = Max.	3.0		V
Logic High	With TTL trip level options	2.0		V
Logic Low	selected, V_{CC} = 5V ± 5%	– 0.3	0.8	V
Logic High	With high trip level options	3.6		V
Logic Low	selected	– 0.3	1.2	V
Input Capacitance			7	pF
Hi-Z Input Leakage		– 1	+ 1	µA
Output Voltage Levels				
LSTTL Operation	V_{CC} = 5V ± 5%			
Logic High (V_{OH})	I_{OH} = – 25µA	2.7		V
Logic Low (V_{OL})	I_{OL} = 0.36mA		0.4	V
CMOS Operation				
Logic High	I_{OH} = – 10µA	V_{CC} – 1		V
Logic Low	I_{OL} = + 10µA		0.2	V

Notes : 1. V_{CC} voltage change must be less than 0.5V in a 1ms period to maintain proper operation.
2. SO output "0" level must be less than 0.8V for normal operation.

ETL9410/ETL9411

DC ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	Min.	Max.	Unit
Output Current Levels				
Output Sink Current				
SO and SK Outputs (I_{OL})	V_{CC} = 9.5V, V_{OL} = 0.4V	1.8		mA
	V_{CC} = 6.3V, V_{OL} = 0.4V	1.2		mA
	V_{CC} = 4.5V, V_{OL} = 0.4V	0.9		mA
L_0-L_7 Outputs G_0-G_3 and LSTTL D_0-D_3 Outputs (I_{OL})	V_{CC} = 9.5V, V_{OL} = 0.4V	0.8		mA
	V_{CC} = 6.3V, V_{OL} = 0.4V	0.5		mA
	V_{CC} = 4.5V, V_{OL} = 0.4V	0.4		mA
D_0-D_3 Outputs with High Current Options (I_{OL})	V_{CC} = 9.5V, V_{OL} = 1.0V	15		mA
	V_{CC} = 6.3V, V_{OL} = 1.0V	11		mA
	V_{CC} = 4.5V, V_{OL} = 1.0V	7.5		mA
D_0-D_3 Outputs with Very High Current Options (I_{OL})	V_{CC} = 9.5V, V_{OL} = 1.0V	30		mA
	V_{CC} = 6.3V, V_{OL} = 1.0V	22		mA
	V_{CC} = 4.5V, V_{OL} = 1.0V	15		mA
CKI (single-pin RC oscillator)	V_{CC} = 4.5V, V_{IH} = 3.5V	2		mA
Output Source Current				
Standard Configuration, All Outputs (I_{OH})	V_{CC} = 9.5V, V_{OH} = 2.0V	– 140	– 800	µA
	V_{CC} = 6.3V, V_{OH} = 2.0V	– 75	– 480	µA
	V_{CC} = 4.5V, V_{OH} = 2.0V	– 30	– 250	µA
Push-pull Configuration SO and SK Outputs (I_{OH})	V_{CC} = 9.5V, V_{OH} = 4.75V	– 1.4		mA
	V_{CC} = 6.3V, V_{OH} = 2.4V	– 1.4		mA
	V_{CC} = 4.5V, V_{OH} = 1.0V	– 1.2		mA
LED Configuration, L_0-L_7 Outputs, Low Current Driver Option (I_{OH})	V_{CC} = 9.5V, V_{OH} = 2.0V	– 1.5	– 18	mA
LED Configuration, L_0-L_7	V_{CC} = 6.0V, V_{OH} = 2.0V	– 1.5	– 13	mA
Outputs, High Current Driver Option (I_{OH})	V_{CC} = 9.5V, V_{OH} = 2.0V	– 3.0	– 35	mA
TRI-STATE® Configuration,	V_{CC} = 6.0V, V_{OH} = 2.0V	– 3.0	– 25	mA
L_0-L_7 Outputs, Low	V_{CC} = 9.5V, V_{OH} = 5.5V	– 0.75		mA
Current Driver Option (I_{OH})	V_{CC} = 6.3V, V_{OH} = 3.2V	– 0.8		mA
TRI-STATE® Configuration,	V_{CC} = 4.5V, V_{OH} = 1.5V	– 0.9		mA
L_0-L_7 Outputs, High	V_{CC} = 9.5V, V_{OH} = 5.5V	– 1.5		mA
Current Driver Option (I_{OH})	V_{CC} = 6.3V, V_{OH} = 3.2V	– 1.6		mA
Input Load Source Current	V_{CC} = 4.5V, V_{OH} = 1.5V	– 1.8		mA
	V_{CC} = 5.0V, V_{IL} = 0V	– 10	– 140	µA
CKO Output				mA
RAM Power Supply Option Power Requirement	V_R = 3.3V		1.5	
TRI-STATE® Output Leakage Current		– 2.5	+ 2.5	µA
Total Sink Current Allowed				
All Outputs Combined			100	mA
D Port			100	mA
L_7-L_4, G Port			4	mA
L_3-L_0			4	mA
Any Other Pin			2.0	mA
Total Source Current Allowed				
All I/O Combined			120	mA
L_7-L_4			60	mA
L_3-L_0			60	mA
Each L Pin			25	mA
Any Other Pin			1.5	mA

ETL9310/ETL9311

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
	Voltage at Any Pin Relative to GND	– 0.5 to + 10	V
	Ambient Operating Temperature	– 40 to + 85	°C
	Ambient Storage Temperature	– 65 to + 150	°C
	Lead Temperature (soldering, 10 seconds)	300	°C
	Power Dissipation ETL9310 ETL9311	0.75W at 25°C 0.25W at 85°C 0.65W at 25°C 0.20W at 85°C	
	Total Source Current	120	mA
	Total Sink Current	100	mA

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC ELECTRICAL CHARACTERISTICS – 40°C ≤ T_A ≤ + 85°C, 4.5V ≤ V_{CC} ≤ 7.5V (unless otherwise specified)

Parameter	Test Conditions	Min.	Max.	Unit
Standard Operating Voltage (V_{CC})	Note 1	4.5	5.5	V
Optional Operating Voltage (V_{CC})		4.5	7.5	V
Power Supply Ripple	Peak to Peak		0.5	V
Operating Supply Current	All Inputs and Outputs Open		8	mA
Input Voltage Levels				
Ceramic Resonator Input (÷8)				
Crystal Input				
Logic High (V_{IH})		2.2		V
Logic Low (V_{IL})		– 0.3	0.3	V
Schmitt Trigger Input (÷4)				
Logic High (V_{IH})		0.7 V_{CC}		V
Logic Low (V_{IL})		– 0.3	0.4	V
$\overline{RESET}$ Input Levels	(schmitt trigger input)			
Logic High		0.7 V_{CC}		V
Logic Low		– 0.3	0.4	V
SO Input Level (test mode)	Note 2	2.2	2.5	V
All Other Inputs				
Logic High	V_{CC} = Max.	3.0		V
Logic High	With TTL trip level options	2.2		V
Logic Low	selected, V_{CC} = 5V ± 5%	– 0.3	0.6	V
Logic High	With high trip level options	3.6		V
Logic Low	selected	– 0.3	1.2	V
Input Capacitance			7	pF
Hi-Z Input Leakage		– 2	+ 2	µA
Output Voltage Levels				
LSTTL Operation	V_{CC} = 5V ± 5%			
Logic High (V_{OH})	I_{OH} = – 20µA	2.7		V
Logic Low (V_{OL})	I_{OL} = 0.36mA		0.4	V
CMOS Operation				
Logic High	I_{OH} = – 10µA	V_{CC} – 1		V
Logic Low	I_{OL} = + 10µA		0.2	V

Notes : 1. V_{CC} voltage change must be less than 0.5V in a 1ms period to maintain proper operation.
2. SO output "0" level must be less than 0.6V for normal operation.

ETL9310/ETL9311

DC ELECTRICAL CHARACTERISTICS (continued)

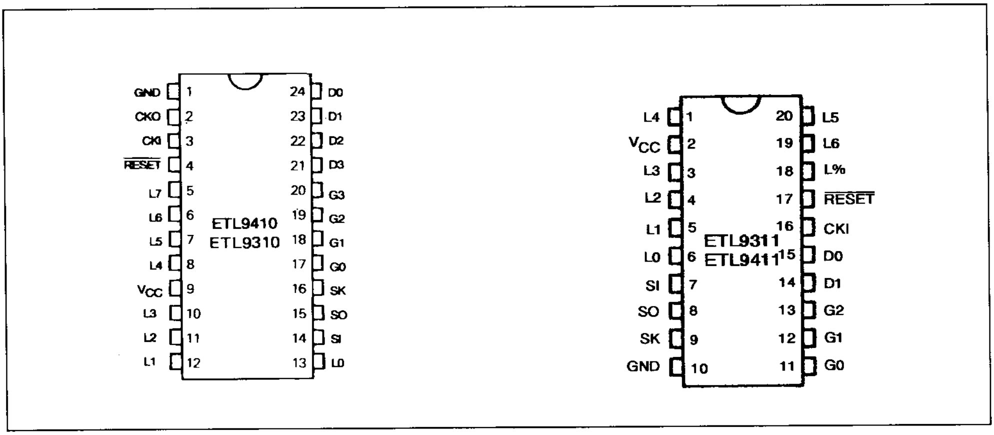
Parameter	Test Conditions	Min.	Max.	Unit
Output Current Levels				
Output Sink Current				
SO and SK Outputs (I_{OL})	V_{CC} = 7.5V, V_{OL} = 0.4V	1.4		mA
	V_{CC} = 5.5V, V_{OL} = 0.4V	1.0		mA
	V_{CC} = 4.5V, V_{OL} = 0.4V	0.8		mA
L_0-L_7 Outputs, G_0-G_3 and	V_{CC} = 7.5V, V_{OL} = 0.4V	0.6		mA
LSTTL, D_0-D_3 Outputs (I_{OL})	V_{CC} = 5.5V, V_{OL} = 0.4V	0.5		mA
	V_{CC} = 4.5V, V_{OL} = 0.4V	0.4		mA
D_0-D_3 Outputs with	V_{CC} = 7.5V, V_{OL} = 1.0V	12		mA
High Current Options (I_{OL})	V_{CC} = 5.5V, V_{OL} = 1.0V	9		mA
	V_{CC} = 4.5V, V_{OL} = 1.0V	7		mA
D_0-D_3 Outputs with	V_{CC} = 7.5V, V_{OL} = 1.0V	24		mA
Very High Current Options (I_{OL})	V_{CC} = 5.5V, V_{OL} = 1.0V	18		mA
	V_{CC} = 4.5V, V_{OL} = 1.0V	14		mA
CKI (single-pin RC oscillator)	V_{CC} = 4.5V, V_{IH} = 3.5V	2		mA
Output Source Current				
Standard Configuration,	V_{CC} = 7.5V, V_{OH} = 2.0V	– 100	– 900	µA
All Outputs (I_{OH})	V_{CC} = 5.5V, V_{OH} = 2.0V	– 55	– 600	µA
	V_{CC} = 4.5V, V_{OH} = 2.0V	– 28	– 350	µA
Push-pull Configuration	V_{CC} = 7.5V, V_{OH} = 3.75V	– 0.85		mA
SO and SK Outputs (I_{OH})	V_{CC} = 5.5V, V_{OH} = 2.0V	– 1.1		mA
	V_{CC} = 4.5V, V_{OH} = 1.0V	– 1.2		mA
LED Configuration, L_0-L_7 Outputs, Low Current Driver Option (I_{OH})	V_{CC} = 7.5V, V_{OH} = 2.0V	– 1.4	– 27	mA
LED Configuration, L_0-L_7 Outputs, High Current Driver Option (I_{OH})	V_{CC} = 7.5V, V_{OH} = 2.0V	– 2.7	– 54	mA
TRI-STATE® Configuration,	V_{CC} = 7.5V, V_{OH} = 4.0V	– 0.7		mA
L_0-L_7 Outputs, Low	V_{CC} = 5.5V, V_{OH} = 2.7V	– 0.6		mA
Current Driver Option (I_{OH})	V_{CC} = 4.5V, V_{OH} = 1.5V	– 0.9		mA
TRI-STATE® Configuration,	V_{CC} = 7.5V, V_{OH} = 4.0V	– 1.4		mA
L_0-L_7 Outputs, High	V_{CC} = 5.5V, V_{OH} = 2.7V	– 1.2		mA
Current Driver Option (I_{OH})	V_{CC} = 4.5V, V_{OH} = 1.5V	– 1.8		mA
Input Load Source Current	V_{CC} = 5.0V, V_{IL} = 0V	– 10	– 200	µA
CKO Output				mA
RAM Power Supply Option				
Power Requirement	V_R = 3.3V		2.0	
TRI-STATE® Output Leakage Current		– 5	+ 5	µA
Total Sink Current Allowed				
All Outputs Combined			100	mA
D Port			100	mA
L_7-L_4, G Port			4	mA
L_3-L_0			4	mA
Any Other Pin			2.0	mA
Total Source Current Allowed				
All I/O Combined			120	mA
L_7-L_4			60	mA
L_3-L_0			60	mA
Each L Pin			25	mA
Any Other Pin			1.5	mA

AC ELECTRICAL CHARACTERISTICS

ETL9410/L9411 : 0°C ≤ T_A ≤ + 70°C, 4.5V ≤ V_{CC} ≤ 9.5V (unless otherwise specified)
ETL9310/L9311 : – 40°C ≤ T_A ≤ + 85°C, 4.5V ≤ V_{CC} ≤ 7.5V (unless otherwise specified)

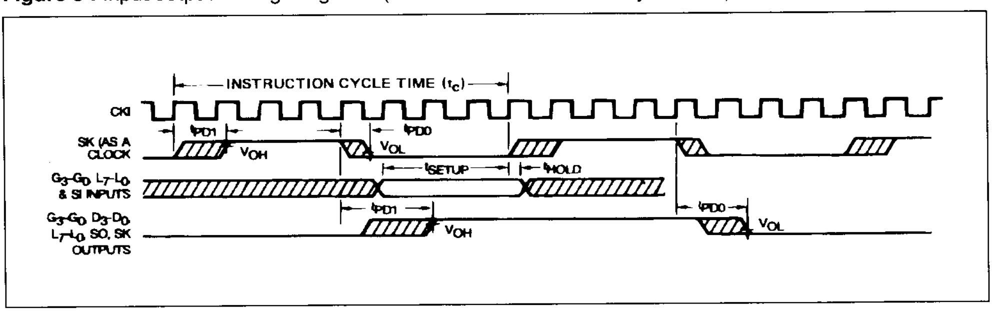
Parameter	Test Conditions	Min.	Max.	Unit
Instruction Cycle Time – t_c		16	40	µs
CKI				
Input Frequency – f_I	÷ 8 Mode	0.2	0.5	MHz
	÷ 4 Mode	0.1	0.25	MHz
Duty Cycle		30	60	%
Rise Time	f_I = 0.5MHz		500	ns
Fall Time			200	ns
CKI Using RC (÷ 4)	R = 56kΩ ± 5% C = 100pF ± 10%			
Instruction Cycle Time		16	28	µs
CKO as SYNC Input				
t_{SYNC}		400		ns
INPUTS :				
G_3-G_0, L_7-L_0				
t_{SETUP}			8.0	µs
t_{HOLD}			1.3	µs
SI				
t_{SETUP}			2.0	µs
t_{HOLD}			1.0	µs
OUTPUT PROPAGATION DELAY	Test Condition : C_L = 50pF, R_L = 20kΩ, V_{OUT} = 1.5V			
SO, SK Outputs				
t_{pd1}, t_{pd0}			4.0	µs
All Other Outputs				
t_{pd1}, t_{pd0}			5.6	µs

Figure 2 : Pin Connection.



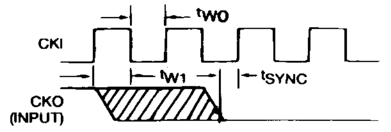
Pin	Description
L_7-L_0	8 Bidirectional I/O Ports with TRI-STATE®
G_3-G_0	4 Bidirectional I/O Ports (G_2-G_0 for COP411L)
D_3-D_0	4 General Purpose Outputs (D_1-D_0 for ETL9411)
SI	Serial Input (or counter input)
SO	Serial Output (or general purpose output)
SK	Logic-controlled Clock (or general purpose output)
CKI	System Oscillator Input
CKO	Crystal Oscillator Output (or RAM power supply or SYNG input) (ETL9410 only)
$\overline{RESET}$	System Reset Input
V_{CC}	Power Supply
GND	Ground

Figure 3 : Input/output Timing Diagrams (ceramic resonator divide-by-8 mode).



SGS-THOMSON MICROELECTRONICS

Figure 3a : Synchronization Timing.



FUNCTIONAL DESCRIPTION

A block diagram of the ETL9410 is given in figure 1. Data paths are illustrated in simplified form to depict how the various logic elements communicate with each other in implementing the instruction set of the device. Positive logic is used. When a bit is set, it is a logic "1" (greater than 2 volts). When a bit is reset, it is a logic "0" (less than 0.8 volts).

All functional references to the ETL9410/L9411 - also apply to the ETL9310/L9311.

PROGRAM MEMORY

Program Memory consists of a 512-byte ROM.

As can be seen by an examination of the ETL9410/L9411 instruction set, these words may be program instructions, program data or ROM addressing data. Because of the special characteristics associated with the JP, JSRP, JID and LQID instructions, ROM must often be thought of as being organized into 8 pages of 64 words each.

ROM addressing is accomplished by a 9-bit PC register. Its binary value selects one of the 512 8-bit words contained in ROM. A new address is loaded into the PC register during each instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential 9-bit binary count value. Two levels of subroutine nesting are implemented by the 9-bit subroutine save registers, SA and SB, providing a last-in, first-out (LIFO) hardware subroutine stack.

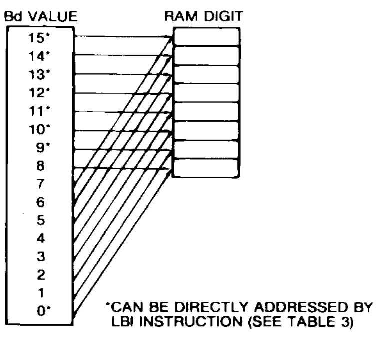
ROM instruction words are fetched, decoded and executed by the instruction Decode, Control and Skip Logic circuitry.

DATA MEMORY

Data memory consists of a 128-bit RAM, organized as 4 data registers of 8 4-bit digits. RAM addressing is implemented by a 6-bit B register whose upper 2 bits (Br) select 1 of 4 data registers and lower 3 bits of the 4-bit Bd select 1 of 8 4-bit digits in the selected data register. While the 4-bit contents of the selected RAM digit (M) is usually loaded into or from, or exchanged with, the A register (accumulator), it may also be loaded into the Q latches or loaded from the L ports. RAM addressing may also be performed directly by the XAD 3, 15 instruction. The Bd register also serves as a source register for 4-bit data sent directly to the D outputs.

The most significant bit of Bd is not used to select a RAM digit. Hence each physical digit of RAM may be selected by two different values of Bd as shown in figure 4 below. The skip condition for XIS and XDS instructions will be true if Bd changes between 0 and 15, but NOT between 7 and 8 (see table 3).

Figure 4 : RAM Digit Address to Physical RAM Digit Mapping.



INTERNAL LOGIC

The 4-bit A register (accumulator) is the source and destination register for most I/O, arithmetic, logic and data memory access operations. It can also be used to load the Bd portion of the B register, to load 4 bits of the 8-bit Q latch data, to input 4 bits of the 8-bit L I/O port data and to perform data exchanges with the SIO register.

A 4-bit adder performs the arithmetic and logic functions of the ETL9410/L9411, storing its results in A. It also outputs a carry bit to the 1-bit C register, most often employed to indicate arithmetic overflow. The C register, in conjunction with the XAS instruction and the EN register, also serves to control the SK output. C can be outputted directly to SK or can enable SK to be a sync clock each instruction cycle time. (see XAS instruction and EN register description, below).

The G register contents are outputs to 4 general-purpose bidirectional I/O ports.

The Q register is an internal, latched, 8-bit register, used to hold data loaded from M and A, as well as 8-bit data from ROM. Its contents are output to the L I/O ports when the L drivers are enabled under program control (see LEI instruction).

The 8 L drivers, when enabled, output the contents of latched Q data to the L I/O ports. Also, the contents of L may be read directly into A and M. L I/O ports can be directly connected to the segments of a multiplexed LED display (using the LED Direct Drive output configuration option) with Q data being outputted to the Sa - Sg and decimal point segments of the display.

The SIO register functions as a 4-bit serial-in/serial-out shift register or as a binary counter depending on the contents of the EN register. (see EN register description, below). Its contents can be exchanged with A, allowing it to input or output a continuous serial data stream. SIO may also be used to provide additional parallel I/O by connecting SO to external serial-in/parallel-out shift registers.

The XAS instruction copies C into the SKL Latch. In the counter mode, SK is the output of SKL in the shift register mode, SK outputs SKL ANDed with internal instruction cycle clock.

The EN register is an internal 4-bit register loaded under program control by the LEI instruction. The state of each bit of this register selects or deselects the particular feature associated with each bit of the EN register (EN_3-EN_0).

1. The least significant bit of the enable register, EN_0, selects the SIO register as either a 4-bit shift register or a 4-bit binary counter. With EN_0 set, SIO is an asynchronous binary counter, *decrementing* its value by one upon each low-going pulse ("1" to "0") occurring on the SI input. Each pulse must be at least two instruction cycles wide. SK outputs the value of SKL. The SO output is equal to the value of EN_3. With EN_0 reset, SIO is a serial shift register shifting left each instruction cycle time. The data present at SI goes into the least significant bit of SIO. SO can be enabled to output the most significant bit of SIO each cycle time. (see 4 below). The SK output becomes a logic-controlled clock.
2. EN_1 is not used. It has no effect on ETL9410, L9411-operation.
3. With EN_2 set, the L drivers are enabled to output the data in Q to the L I/O ports. Resetting EN_2 disables the L drivers, placing the L I/O ports in a high-impedance input state.
4. En_3, in conjunction with EN_0, affects the SO output. With EN_0 set (binary counter option selected) SO will output the value loaded into EN_3. With EN_0 reset (serial shift register option selected), setting EN_3 enables SO as the output of the SIO shift register, outputting serial shifted data each instruction time. Resetting EN_3 with the serial shift register option selected disables SO as the shift register output ; data continues to be shifted through SIO and can be exchanged with A via an XAS instruction but SO remains reset to "0". Table 1 provides a summary of the modes associated with EN_3 and EN_0.

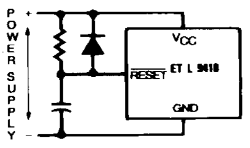
Enable Register Modes - Bits EN_3 and EN_0

EN_3	EN_0	SIO	SI	SO	SK
0	0	Shift Register	Input to Shift Register	0	If SKL = 1, SK = clock If SKL = 0, SK = 0
1	0	Shift Register	Input to Shift Register	Serial Out	If SKL = 1, SK = clock If SKL = 0, SK = 0
0	1	Binary Counter	Input to Binary Counter	0	If SKL = 1, SK = 1 If SKL = 0, SK = 0
1	1	Binary Counter	Input to Binary Counter	1	If SKL = 1, SK = 1 If SKL = 0, SK = 0

INITIALIZATION

The Reset Logic will initialize (clear) the device upon power-up if the power supply rise time is less than 1ms and greater than 1µs. If the power supply rise time is greater than 1ms, the user must provide an external RC network and diode to the RESET pin as shown below (figure 5). The RESET pin is configured as a Schmitt trigger input. If not used it should be connected to V_{CC}. Initialization will occur whenever a logic "0" is applied to the RESET input, provided it stays low for at least three instruction cycle times.

Figure 5 : Power-up Clear Circuit.



RC ≥ 5 x POWER SUPPLY RISE TIME

Upon initialization, the PC register is cleared to 0 (ROM address 0) and the A, B, C, D, EN, and G registers are cleared. The SK output is enabled as a SYNC output, providing a pulse each instruction cycle time. *Data Memory (RAM) is not cleared upon initialization.* The first instruction at address 0 must be a CLRA.

OSCILLATOR

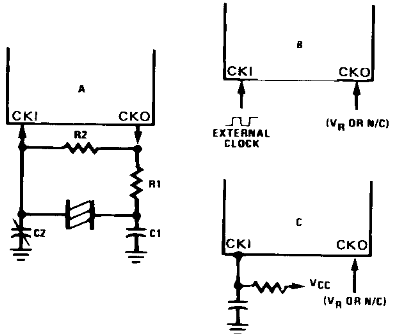
There are three basic clock oscillator configurations available as shown by figure 6.

a. Resonator Controlled Oscillator. CKI and CKO are connected to an external ceramic resonator. The instruction cycle frequency equals the resonator frequency divided by 8. This is not available in the ETL9411.

b. External Oscillator. CKI is an external clock input signal. The external frequency is divided by 8 to give the instruction frequency time. CKO is now available to be used as the RAM power supply (V_R), as a SYNC input, or no connection. (Note : No CKO on ETL9411.

c. RC Controlled Oscillator. CKI is configured as a single pin RC controlled Schmitt trigger oscillator. The instruction cycle equals the oscillation frequency divided by 4. CKO is available as the RAM power supply (V_R) or no connection.

Figure 6 : ETL9410/L9411 Oscillator.



CERAMIC RESONATOR OSCILLATOR

Resonator Value	Component Values			
	R1 (Ω)	R2 (Ω)	C1 (pF)	C2 (pF)
455kHz	1k	1M	80	80

This circuit and these values are for indication only. As the oscillator characteristics are not guaranteed, please consider and examine the circuit constants carefully on your application.

CKO PIN OPTIONS

In a resonator controlled oscillator system, CKO is used as an output to the resonator network. As an option CKO can be a SYNC input as described above. As another option, CKO can be a RAM power supply pin (V_R), allowing its connection to a standby/backup power supply to maintain the integrity of RAM data with minimum power drain when the main supply is inoperative or shut down to conserve power. Using no connection option is appropriate in applications where the ETL9410 system timing configuration does not require use of the CKO pin.

RAM KEEP-ALIVE OPTION

Selecting CKO as the RAM power supply (V_R) allows the user to shut off the chip power supply (V_{CC}) and maintain data in the RAM. To insure that RAM data integrity is maintained, the following conditions must be met :

1. $\overline{RESET}$ must go low before V_{CC} goes below spec during power-off ; V_{CC} must be within spec before $\overline{RESET}$ goes high on power-up.
2. During normal operation, V_R must be within the operating range of the chip with $(V_{CC} - 1) \leq V_R \leq V_{CC}$.
3. V_R must be ≥ 3.3V with V_{CC} off.

RC CONTROLLED OSCILLATOR

R (kΩ)	C (pF)	Instruction Cycle Time in (µs)
51	100	19 ± 15%
82	56	19 ± 13%

Note : 200kΩ ≥ R ≥ 25kΩ.
360pF ≥ C ≥ 50pF.

I/O OPTIONS

ETL9410/L9411 inputs and outputs have the following optional configurations, illustrated in figure 7.

a. Standard - an enhancement mode device to ground in conjunction with a depletion-mode device to V_{CC}, compatible with LSTTL and CMOS input requirements. Available on SO, SK, and all D and G outputs.

b. Open-Drain - an enhancement-mode device to ground only, allowing external pull-up as required by the user's application. Available on SO, SK, and all D and G outputs.

c. Push-Pull - an enhancement-mode device to ground in conjunction with a depletion-mode device paralleled by an enhancement-mode device to V_{CC}. This configuration has been provided to allow for fast rise and fall times when driving capacitive loads. Available on SO and SK outputs only.

d. Standard L - same as a., but may be disabled. Available on L outputs only.

e. Open Drain L - same as b., but may be disabled. Available on L outputs only.

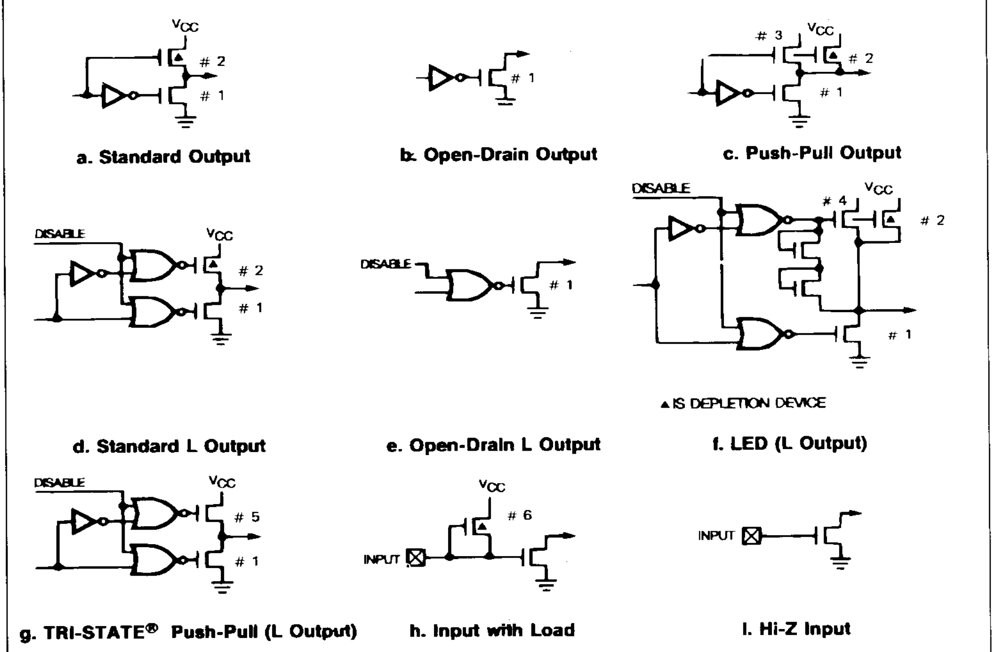
f. LED Direct Drive - an enhancement mode device to ground and to V_{CC}, meeting the typical current sourcing requirements of the segments of an LED display. The sourcing device is clamped to limit current flow. These devices may be turned off under program control (see Functional Description, EN Register), placing the outputs in a high-impedance state to provide required LED segment blanking for a multiplexed display. Available on L outputs only.

g. TRI-STATE® Push-Pull - an enhancement-mode device to ground and V_{CC}. These outputs are TRI-STATE® outputs, allowing for connection of these outputs to a data bus shared by other bus drivers. Available on L outputs only.

h. An on-chip depletion load device to V_{CC}.

i. A Hi-Z input which must be driven to a "1" or "0" by external components.

Figure 7 : Input and Output Configurations.



The above input and output configurations share common enhancement-mode and depletion-mode devices. Specifically, all configurations use one or more of six devices (numbered 1-6, respectively). Minimum and maximum current (I_{OUT} and V_{OUT}) curves are given in figure 8 for each of these devices to allow the designer to effectively use these I/O configurations in designing a ETL9410/L9411 system.

The SO, SK outputs can be configured as shown in a., b., or c. The D and G outputs can be configured as shown in a., or b. Note that when inputting data to the G ports, the G outputs should be set to "1". The L outputs can be configured as in d., e., f., or g.

An important point to remember if using configuration d. or f. with the L drivers is that even when the L drivers are disabled, the depletion load device will source a small amount of current. (see figure 8, device 2). However, when the L port is used as input, the disabled depletion device CANNOT be relied on to source sufficient current to pull an input to a logic "1".

ETL9411

If the ETL9410 is bonded as a 20-pin device, it becomes the ETL9411, illustrated in figure 2, ETL9410/ETL9411 Connection Diagrams. Note that the ETL9411 does not contain D2, D3, G3 or CKO. Use of this option of course precludes use of D2, D3, G3, and CKO options. All other options are available for the ETL9411.

TYPICAL PERFORMANCE CURVES

Figure 8a : ETL9410/L9411 - I/O DC Current Characteristics.

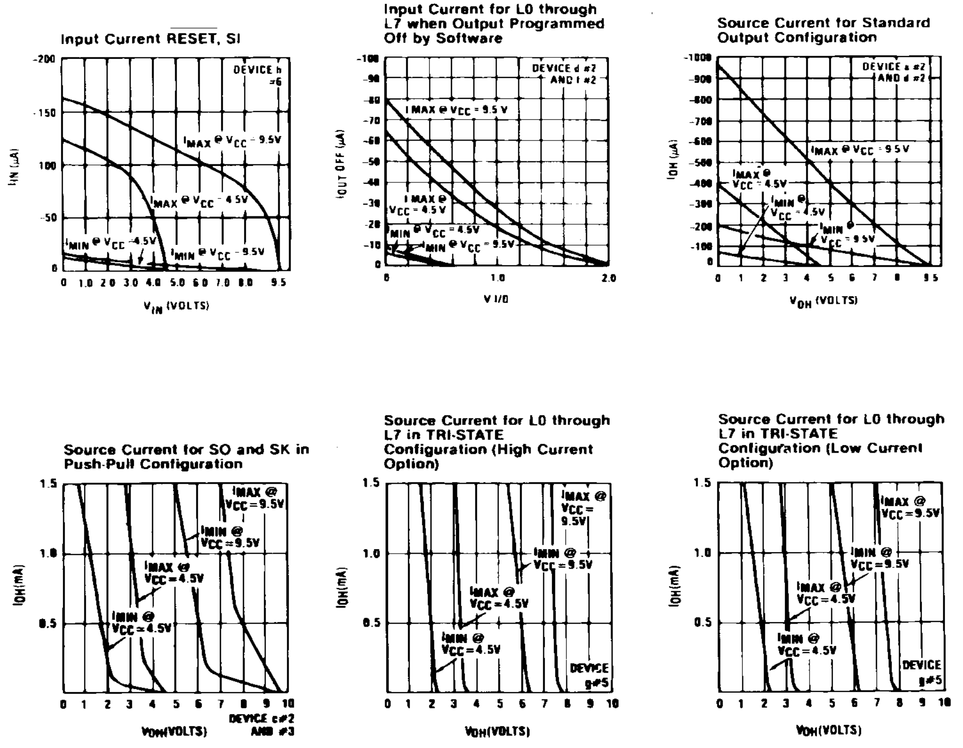
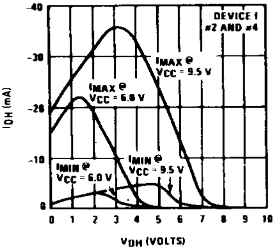
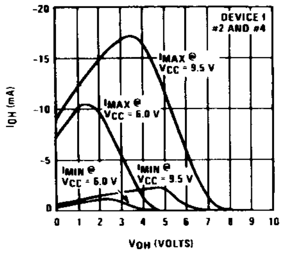


Figure 8a : ETL9410/L9411 - I/O DC Current Characteristics (continued).

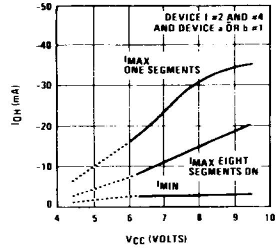
LED Output Source Current (for High Current LED Option)



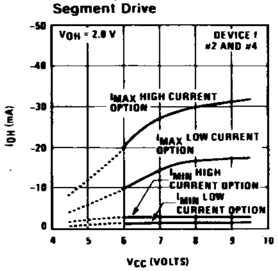
LED Output Source Current (for Low Current LED Option)



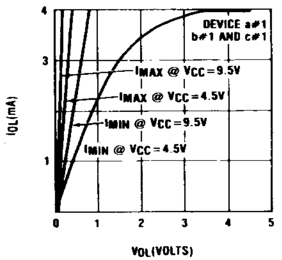
LED Output Direct Segment and Digit Drive
High Current Options on L0-L7
Very High Current Options on D0-D3



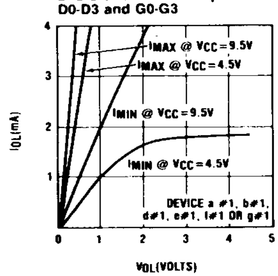
LED Output Direct Segment Drive



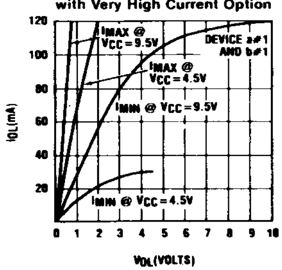
Output Sink Current for SO and SK



Output Sink Current for L0-L7 and Standard Drive Option for D0-D3 and G0-G3



Output Sink Current for D0-D3 with Very High Current Option



Output Sink Current for D0-D3 (for High Current Option)

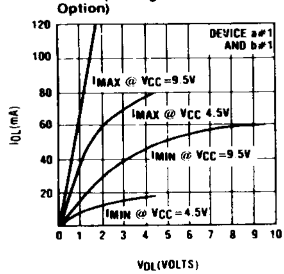
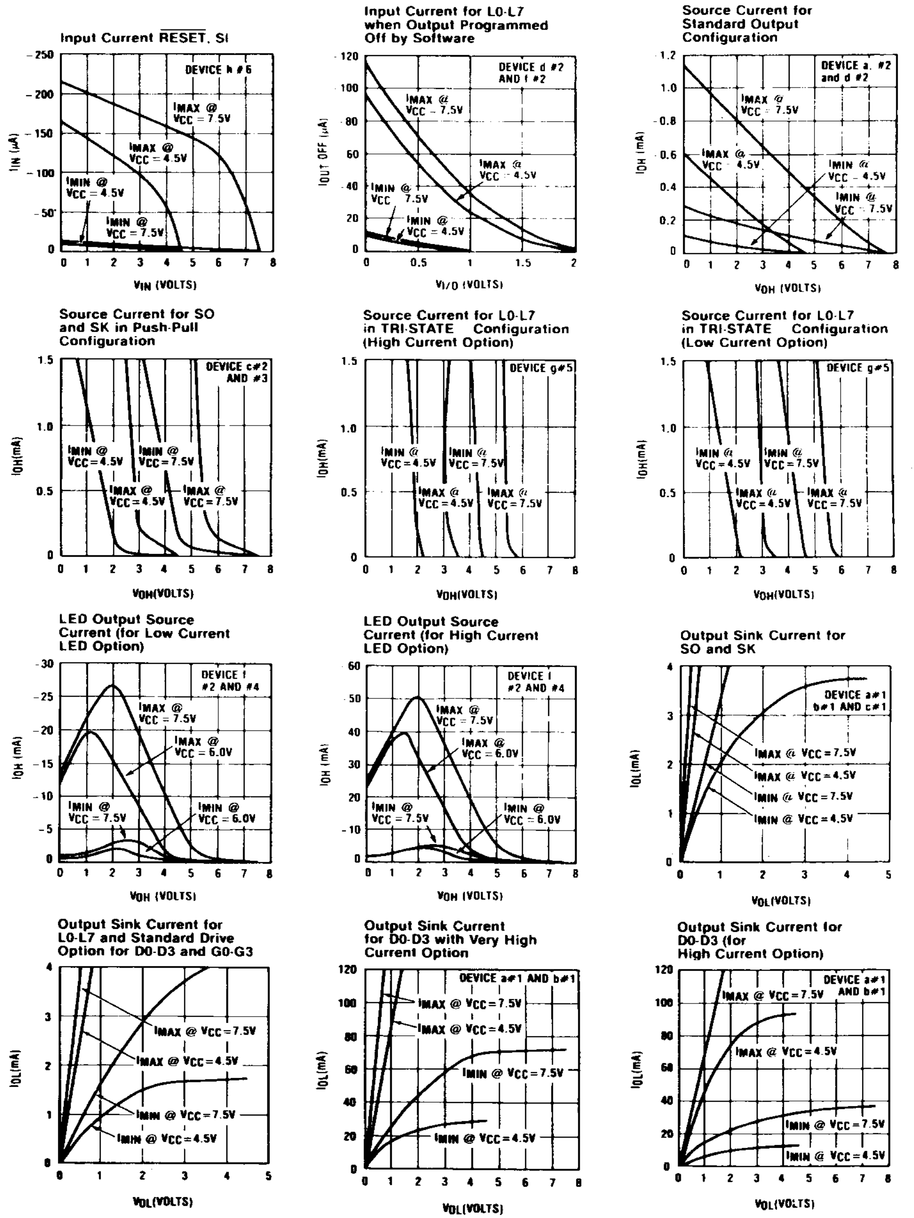


Figure 8b : ETL9310/L9311 Input/output Characteristics.



ETL9410/I9411 - INSTRUCTION SET

Table 2 is a symbol table providing internal architecture, instruction operand and operational symbols used in the instruction set table.

Table 3 provides the mnemonic, operand, machine, code, data flow, skip conditions and description associated with each instruction in the ETL9410/L9411 - instruction set.

Table 2 : ETL9410/L9411 - Instruction Set Table Symbols.

INTERNAL ARCHITECTURE SYMBOLS

Symbol	Definition
A	4-bit Accumulator
B	6-bit RAM Address Register
Br	Upper 2 Bits of B (register address)
Bd	Lower 4 Bits of B (digit address)
C	1-bit Carry Register
D	4-bit Data Output Port
EN	4-bit Enable Register
G	4-bit Register to Latch Data for G I/O Port
L	8-bit TRI-STATE I/O Port
M	4-bit contents of RAM memory pointed to by B register.
PC	9-bit ROM Address Register (program counter)
Q	8-bit Register to Latch Data for L I/O Port
SA	9-bit Subroutine Save Register A
SB	9-bit Subroutine Save Register B
SIO	4-bit Shift Register and Counter
SK	Logic-controlled Clock Output

INSTRUCTION OPERAND SYMBOLS

Symbol	Definition
d	4-bit Operand Field, 0-15 Binary (RAM digit select)
r	2-bit Operand Field, 0-3 Binary (RAM register select)
a	9-bit Operand Field, 0-511 Binary (ROM address)
y	4-bit Operand Field, 0-15 Binary (immediate data)
$RAM_{(s)}$	Contents of RAM location addressed by s.
$ROM_{(t)}$	Contents of ROM location addressed by t.

OPERATIONAL SYMBOLS

Symbol	Definition
+	Plus
–	Minus
→	Replaces
↔	Is exchanged with.
=	Is equal to.
$\overline{A}$	The one's complement of A
⊕	Exclusive-OR
:	Range of Values

Table 3 : ETL9410/L9411 - Instruction Set.

ARITHMETIC INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
ASC		30	0011 | 0000	A + C + RAM(B) → A Carry → C	Carry	Add with Carry, Skip on Carry
ADD		31	0011 | 0001	A + RAM(B) → A	None	Add RAM to A
AISC	y	5–	0101 | y	A + y → A	Carry	Add Immediate, Skip on Carry (y ≠ 0)
CLRA		00	0000 | 0000	0 → A	None	Clear A
COMP		40	0100 | 0000	$\overline{A}$ → A	None	One's Complement of A to A
NOP		44	0100 | 0100	None	None	No Operation
RC		32	0011 | 0010	"0" → C	None	Reset C
SC		22	0010 | 0010	"1" → C	None	Set C
XOR		02	0000 | 0010	A ⊕ RAM(B) → A	None	Exclusive-OR RAM with A

TRANSFER OF CONTROL INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
JID		FF	1111 | 1111	ROM(PC_8 A, M) $\rightarrow PC_{7:0}$	None	Jump Indirect (note 2)
JMP	a	6–	0110 | 000 | a_8 $a_{7:0}$	$a \rightarrow PC$	None	Jump
JP	a		1 | $a_{6:0}$ (pages 2,3 only) or 11 | $a_{5:0}$ (all other pages)	$a \rightarrow PC_{6:0}$ $a \rightarrow PC_{5:0}$	None	Jump within Page (note 3)
JSRP	a		10 | $a_{5:0}$	$PC + 1 \rightarrow SA \rightarrow SB$ $010 \rightarrow PC_{8:6}$ $a \rightarrow PC_{5:0}$	None	Jump to Subroutine Page (note 4)
JSR	a	6–	0110 | 100 | a_8 $a_{7:0}$	$PC + 1 \rightarrow SA \rightarrow SB$ $a \rightarrow PC$	None	Jump to Subroutine
RET		48	0100 | 1000	$SB \rightarrow SA \rightarrow PC$	None	Return from Subroutine
RETSK		49	0100 | 1001	$SB \rightarrow SA \rightarrow PC$	Always Skip on Return	Return from Subroutine then Skip

MEMORY REFERENCE INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
CAMQ		33 3C	0011 | 0011 0011 | 1100	$A \rightarrow Q_{7:4}$ RAM(B) $\rightarrow Q_{3:0}$	None	Copy A, RAM to Q
LD	r	–5	00 | r | 0101	RAM(B) $\rightarrow$ A $Br \oplus r \rightarrow Br$	None	Load RAM into A, Exclusive-OR Br with r
LQID		BF	1011 | 1111	ROM(PC_8, A, M) $\rightarrow$ Q $SA \rightarrow SB$	None	Load Q Indirect (note 2)
RMB	0 1 2 3	4C 45 42 43	0100 | 1100 0100 | 0101 0100 | 0010 0100 | 0011	$0 \rightarrow RAM(B)_0$ $0 \rightarrow RAM(B)_1$ $0 \rightarrow RAM(B)_2$ $0 \rightarrow RAM(B)_3$	None	Reset RAM Bit
SMB	0 1 2 3	4D 47 46 4B	0100 | 1101 0100 | 0111 0100 | 0110 0100 | 1011	$1 \rightarrow RAM(B)_0$ $1 \rightarrow RAM(B)_1$ $1 \rightarrow RAM(B)_2$ $1 \rightarrow RAM(B)_3$	None	Set RAM Bit
STII	y	7–	0111 | y	$y \rightarrow$ RAM(B) $Bd + 1 \rightarrow Bd$	None	Store Memory Immediate and Increment Bd
X	r	–6	00 | r | 0110	RAM(B) $\leftrightarrow$ A $Br \oplus r \rightarrow Br$	None	Exchange RAM with A, Exclusive-OR Br with r
XAD	3,15	23 BF	0010 | 0011 1011 | 1111	RAM(3,15) $\leftrightarrow$ A	None	Exchange A with RAM (3,15)

MEMORY REFERENCE INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
XDS	r	–7	| 0 0 | r | 0 1 1 1 |	RAM(B) ↔ A Bd – 1 → Bd Br ⊕ r → Br	Bd Decrements Past 0	Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r
XIS	r	–4	| 0 0 | r | 0 1 0 0 |	RAM(B) ↔ A Bd + 1 → Bd Br ⊕ r → Br	Bd Increments Past 15	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r

REGISTER REFERENCE INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
CAB		50	| 0 1 0 1 | 0 0 0 0 |	A → Bd	None	Copy A to Bd
CBA		4E	| 0 1 0 0 | 1 1 1 0 |	Bd → A	None	Copy Bd to A
LBI	r,d		| 0 0 | r | (d-1) | (d = 0.9:15)	r,d → B	Skip until not a LBI	Load B Immediate with r,d (note 5)
LEI	y	33 6–	| 0 0 1 1 | 0 0 1 1 | | 0 1 1 0 | y |	y → EN	None	Load EN Immediate (note 6)

TEST INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
SKC		20	| 0 0 1 0 | 0 0 0 0 |		C = "1"	Skip if C is true.
SKE		21	| 0 0 1 0 | 0 0 0 1 |		A = RAM(B)	Skip if A Equals RAM
SKGZ		33 21	| 0 0 1 1 | 0 0 1 1 | | 0 0 1 0 | 0 0 0 1 |		$G_{3:0} = 0$	Skip if G is zero (all 4 bits).
SKGBZ	 0 1 2 3	33 01 11 03 13	| 0 0 1 1 | 0 0 1 1 | | 0 0 0 0 | 0 0 0 1 | | 0 0 0 1 | 0 0 0 1 | | 0 0 0 0 | 0 0 1 1 | | 0 0 0 1 | 0 0 1 1 |	1st Byte 2nd Byte	 $G_0 = 0$ $G_1 = 0$ $G_2 = 0$ $G_3 = 0$	Skip if G Bit is zero.
SKMBZ	0 1 2 3	01 11 03 13	| 0 0 0 0 | 0 0 0 1 | | 0 0 0 1 | 0 0 0 1 | | 0 0 0 0 | 0 0 1 1 | | 0 0 0 1 | 0 0 1 1 |		$RAM(B)_0 = 0$ $RAM(B)_1 = 0$ $RAM(B)_2 = 0$ $RAM(B)_3 = 0$	Skip if RAM bit is zero.

INPUT/OUTPUT INSTRUCTIONS

Mnem	Operand	Hex Code	Machine Language Code (binary)	Data Flow	Skip Conditions	Description
ING		33 2A	|0 0 1 1|0 0 1 1| |0 0 1 0|1 0 1 0|	$G \rightarrow A$	None	Input G Ports to A
INL		33 2E	|0 0 1 1|0 0 1 1| |0 0 1 0|1 1 1 0|	$L_{7:4} \rightarrow$ RAMB(B) $L_{3:0} \rightarrow A$	None	Input L Ports to RAM, A
OBD		33 3E	|0 0 1 1|0 0 1 1| |0 0 1 1|1 1 1 0|	Bd $\rightarrow$ D	None	Output Bd to D Outputs
OMG		33 3A	|0 0 1 1|0 0 1 1| |0 0 1 1|1 0 1 0|	RAM(B) $\rightarrow$ G	None	Output RAM to G Ports
XAS		4F	|0 1 0 0|1 1 1 1|	A $\leftrightarrow$ SIO, C $\rightarrow$ SKL	None	Exchange A with SIO (note 2)

Notes :

1. All subscripts for alphabetical symbols indicate bit numbers unless explicitly defined (e.g., Br and Bd are explicitly defined). Bits are numbered 0 to N where 0 signifies the least significant bit (low-order, right-most bit). For example, A_3 indicates the most significant (left-most) bit of the 4-bit A register.
2. For additional information on the operation of the XAS, JID, and LQID instructions, see below.
3. The JP instruction allows a jump, while in subroutine pages 2 or 3, to any ROM location within the two-page boundary of pages 2 or 3. The JP instruction, otherwise, permits a jump to a ROM location within the current 64-word page. JP may not jump to the last word of a page.
4. A JSRP transfers program control to subroutine page 2 (0010 is loaded into the upper 4 bits of P). A JSRP may not be used when in pages 2 or 3. JSRP may not jump to the last word in page 2.
5. The machine code for the lower 4 bits of the LBI instruction equals the binary value of the "d" *data minus* 1, e.g., to load the lower four bits of B (Bd) with the value 9 (1001_2), the lower 4 bits of the LBI instruction equal 8 (1000_2). To load 0, the lower 4 bits of the LBI instruction should equal 15 (11112).
6. Machine code for operand field y for LEI instruction should equal the binary value to be latched into EN, where a "1" or "0" in each bit of EN corresponds with the selection or deselection of a particular function associated with each bit. (see Functional Description, EN Register).

The following information is provided to assist the user in understanding the operation of several unique instructions and to provide notes useful to programmers in writing ETL9410/L9411.

XAS INSTRUCTION

XAS (Exchange A with SIO) exchanges the 4-bit contents of the accumulator with the 4-bit contents of the SIO register. The contents of SIO will contain serial-in/serial-out shift register or binary counter data, depending on the value of the EN register. An XAS instruction will also affect the SK output. (see Functional Description, EN Register, above). If SIO is selected as a shift register, an XAS instruction must be performed once every 4 instruction cycles to effect a continuous data stream.

JID INSTRUCTION

JID (Jump Indirect) is an indirect addressing instruction, transferring program control to a new ROM location pointed to indirectly by A and M. It loads the lower 8 bits of the ROM address register PC with the *contents* of ROM addressed by the 9-bit word, PC_8, A, M. PC_8 is not affected by this instruction.

Note that JID requires 2 instruction cycles to execute.

LQID INSTRUCTION

LQID (Load Q Indirect) loads the 8-bit Q register with the contents of ROM pointed to by the 9-bit word PC_8, A, M. LQID can be used for table lookup or code conversion such as BCD to seven-segment. The LQID instruction "pushes" the stack (PC + 1→SA→SB) and replaces the least significant 8 bits of PC as follows : A→$PC_{7:4}$, RAM(B)→$PC_{3:0}$, leaving PC_8 unchanged. The ROM data pointed to by the new address is fetched and loaded into the Q latches. Next, the stack is "popped" (SB→A→PC), restoring the saved value of PC to continue sequential program execution. Since LQID pushes SA→SB, the previous contents of SB are lost. Also, when LQID pops the stack, the previously pushed contents of SA are left in SB. The net result is that the contents of SA are placed in SB (SA → SB). Note that LQID takes two instruction cycle times to execute.

INSTRUCTION SET NOTES

a. The first word of a ETL9410/ETL9411 program (ROM address 0) must be a CLRA (Clear A) instruction.

b. Although skipped instructions are not executed, one instruction cycle time is devoted to skipping each byte of the skipped instruction. Thus all program paths except JID and LQID take the same number of cycle times whether instructions are skipped or executed. JID and LQID instructions take 2 cycles if executed and 1 cycle if skipped.

c. The ROM is organized into 8 pages of 64 words each. The Program Counter is a 9-bit binary counter, and will count through page boundaries. If a JP, JSRP, JID or LQID instruction is located in the last word of a page, the instruction operates as if it were in the next page. For example : a JP located in the last word of a page will jump to a location in the next page. Also, a LQID or JID located in the last word of page 3 or 7 will access data in the next group of 4 pages.

OPTION LIST

The ETL9410/ETL9411 - mask programmable options are assigned numbers which correspond with the ETL9410 pins.

The following is a list of ETL9410 options. When specifying a ETL9411 chip, Option 2 must be set to 3, Options 20, 21, and 22 to 0. The options are programmed at the same time as the ROM pattern to provide the user with the hardware flexibility to interface to various I/O components using little or no external circuitry.

Option 1 = 0 : Ground Pin - no options available

Option 2 : CKO Output (no option available for ETL9411)
= 0 : Clock output to ceramic resonator
= 1 : Pin is RAM power supply (V_R) input
= 3 : No connection

Option 3 : CKI Input
= 0 : Oscillator input divided by 8 (500kHz max.)
= 1 : Single-pin RC controlled oscillator divided by 4
= 2 : External Schmitt trigger level clock divided by 4

Option 4 : $\overline{\text{RESET}}$ Input
= 0 : Load device to V_{CC}
= 1 : Hi-Z input

Option 5 : L_7 Driver
= 0 : Standard output
= 1 : Open-drain output
= 2 : High current LED direct segment drive output
= 3 : High current TRI-STATE® push-pull output
= 4 : Low-current LED direct segment drive output
= 5 : Low-current TRI-STATE® push-pull output

Option 6 : L_6 Driver
same as Option 5

Option 7 : L_5 Driver
same as Option 5

Option 8 : L_4 Driver
same as Option 5

Option 9 : V_{CC} Pin
= 0 : 4.5V to 6.3V operation
= 1 : 4.5V to 9.5V operation

Option 10 : L_3 Driver
same as Option 5

Option 11 : L_2 Driver
same as Option 5

Option 12 : L_1 Driver
same as Option 5

Option 13 : L_0 Driver
same as Option 5

Option 14 : SI Input
= 0 : load device to V_{CC}
= 1 : Hi-Z input

Option 15 : SO Driver
= 0 : Standard Output
= 1 : Open-drain output
= 2 : Push-pull output

Option 16 : SK Driver
same as Option 15

Option 17 : G_0 I/O Port
= 0 : Standard output
= 1 : Open-drain output

Option 18 : G_1 I/O Port
same as Option 17

Option 19 : G_2 I/O Port
same as Option 17

Option 20 : G_3 I/O Port (no option available for ETL9411)
same as Option 17

Option 21 : D_3 Output (no option available for ETL9411)
= 0 : Very-high sink current standard output
= 1 : Very-high sink current open-drain output
= 2 : High sink current standard output
= 3 : High sink current open-drain output
= 4 : Standard LSTTL output (fanout = 1)
= 5 : Open-drain LSTTL output (fanout = 1)

Option 22 : D_2 Output (no option available for ETL9411)
same as Option 21

Option 23 : D_1 Output
same as Option 21

Option 24 : D_0 Output
same as Option 21

Option 25 : L Input Levels
= 0 : Standard TTL input levels ("0" = 0.8V, "1" = 2.0V)
= 1 : Higher voltage input levels ("0" = 1.2V, "1" = 3.6V)

Option 26 : G Input Levels
same as Option 25

Option 27 : SI Input Levels
same as Option 25

Option 28 : Bonding

= 0 : ETL9410 (24-pin device)
= 1 : ETL9411 (20-pin device)
= 2 : Both 24- and 20-pin versions

TEST MODE (non-standard operation)

The SO output has been configured to provide for standard test procedures for the custom-programmed ETL9410. With SO forced to logic "1", two test modes are provided, depending upon the value of SI :

a. RAM and Internal Logic Test Mode (SI = 1)

b. ROM Test Mode (SI = 0)

These special test modes should not be employed by the user ; they are intended for manufacturing test only.

PHYSICAL DIMENSIONS

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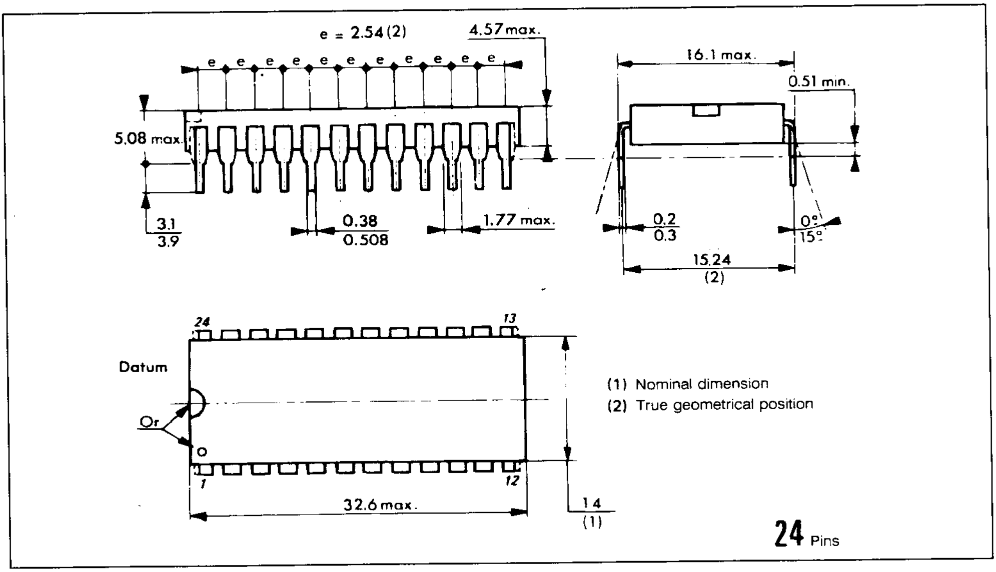

20–PINS – PLASTIC PACKAGE